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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,843	10/08/2004	Kevin Lin	61994.00018	5842

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PATENT DEPARTMENT
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EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
09/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,843	LIN, KEVIN	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/09/07 has been entered.

Status of Claims

Claims 1 – 20 are pending in the Application.

Claims 1, 6, 12, & 17 have been amended.

Claims 1 – 20 are rejected.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 20 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Michigami*** (US 6,223,322).

In regard to claim 1, Michigami teaches generating a block index for a block of data ***(figure 5 "LOGICAL MAPPING")***; mapping the block index to a physical address of a memory based on the block index and a number N, wherein N is bank number of the memory ***(figure 5)***; storing the block of data into the memory at the physical address ***(figure 5 "PHYSICAL MAPPING")***; and looping to the generating step, wherein the mapping step makes each one of the block indexes at all times map in turns to one physical address located at different unconnected banks, and result in any logical adjacent block of data be stored physically at different unconnected banks of the memory ***(col. 6, lines 32 – 44)***.

In regard to claim 17, Michigami teaches generating a plurality of block indexes for a plurality of blocks of data ***(figure 5 "LOGICAL MAPPING")***; mapping the block indexes sequentially to a plurality of physical address of a memory based on the block indexes and a number N, wherein N is bank number of the memory ***(figure 5)***; and storing the block of data into the memory at the physical address ***(figure 5 "PHYSICAL MAPPING")***, wherein the mapping step makes each one of the block indexes at all times map in turns to one physical address located at different unconnected banks, and result in any logical adjacent block of data be stored physically at different unconnected banks of the memory ***(col. 6, lines 32 – 44)***.

In regard to claim 6, Michigami teaches retrieving a block of data from a source media ***(Abstract)***; assigning a block index for the block of data ***(figure 5 "LOGICAL MAPPING")***; dividing value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is bank number of the memory; calculating the physical address based on Q and R ***(col. 6, lines 32***

– ***44; figure 5)***; storing the block of data in the memory at the physical address ***(figure 5 "PHYSCICAL MAPPING")***; and repeating form the retrieving step, wherein the calculating step makes the block index interleaved at all times mapping to the physical address located at different unconnected banks and any two logically successive blocks of data be stored physically at different unconnected banks of the memory ***(col. 6, lines 32 – 44)***.

In regard to claim 12, Michigami teaches means for generating a block index for the block of data ***(figure 5 "LOGICAL MAPPING")***; means for dividing value of the block index by N for acquiring a quotient Q and a reminder R, wherein N is bank number of the memory ***(col. 6, lines 32 – 44)***; and means for calculating the physical address based on Q and R ***(figure 5)***, wherein the calculating means makes the block index interleaved at all times mapping to the physical address located at different unconnected banks and any two logically successive blocks of data be stored physically at different unconnected banks of the memory ***(col. 6, lines 32 – 44)***.

Regarding claims 2, 7, 13, & 18, Michigami teaches wherein the memory supports pipelining access ***(col. 4, lines 12 – 15)***.

Regarding claims 3, 8, 14, & 19, Michigami teaches wherein the memory is a SDRAM ***(fig. 4, element 18)***.

Regarding claims 4 – 5, 9 – 10, 15 – 16, & 20, Michigami teaches dividing the block index by N to obtain a quotient Q and a remainder R ***(col. 6, lines 32 – 44)***; and calculating the physical address based on Q and R, wherein the physical address=Q*block_size+R*bank_size wherein bank_size equals the memory size divided by N, and block_size equals the size of which the system is in need to process one sector from the optical disc ***(figure 5)***.

Regarding claim 11, Michigami teaches reading the block of data according to the block index and the reference function; ***(figure 5)*** and recording the block of data to a destination media, whereby the reading step makes each one of the block of data read at different banks in turns and result in time saving and reduces pre-charge overloads by reading in one bank and pre-charge in another bank accessed just before ***(col. 6, lines 32 – 44; col. 5, lines 41 – 50)***.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Buckelew (US 6,278,645) teaches a high-speed video frame buffer that accesses one memory bank while the other is precharging.

Lee (US 6,745,277) teaches intelligent interleaving for multibank memory that allows precharging of one memory bank while the other is being accessed.

Examiner's Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SE

Shawn Eland
09/17/2007

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER
9/17/07